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10/735,048	12/15/2003	Jun Koyama	740756-2674	2504

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EXAMINER	
NGUYEN, KIMNHUNG T	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,048	KOYAMA, JUN	
	Examiner	Art Unit	
	Kimnhung Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/15/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined. The claims 1-20 are pending. The examination results are following.

DETAILED ACTION

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-16 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 2001/007447).

As to claim 1, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix, each of the pixels comprising:

a switching element (see TFT);

a nonvolatile memory element; and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line (see TFT connected to Y1-Ym);

an output terminal of the switching element is electrically connected to the pixel electrode; and

a control terminal of the switching element is electrically connected to the gate signal line.

However, fig. 12 does not disclose a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the nonvolatile memory element (3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element of fig. 1 of Tanaka et al. into the fig. 12 of prior art for producing the claimed invention because this would be composed of a ferroelectric capacitor and can hold the control data of the MOS transistor in a floating state (see 0033).

As to claim 2, Tanaka et al. discloses in fig. 12, a display device comprising:

A plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising a plurality of sub-pixels, each of the sub-pixels comprising:

a switching element (TFT); and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the pixel electrode; and

a control terminal of the switching element is electrically connected to the gate signal line.

However, Tanaka et al. does not disclose a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 3, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising a plurality of sub-pixels, each of the sub-pixels comprising:

a switching element (see TFT); and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the pixel electrode;

a control terminal of the switching element is electrically connected to the gate signal line; and

each switching element in one of the pixels is electrically connected to different one of the

source signal lines.

However, Tanaka et al. does not disclose a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 4, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising n sub-pixels, each of the sub-pixels comprising:

a switching element; and

a pixel electrode,

wherein:

n lines of the source signal lines are corresponding to one pixel column;

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the pixel electrode; and

a control terminal of the switching element is electrically connected to the gate signal line;

each switching element in one of the pixels is electrically connected to corresponding one of the n lines of the source signal lines.

However, Tanaka et al. does not disclose a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 5, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines X1-Xn); and

a plurality of pixels arranged in matrix comprising a plurality of sub-pixels, each of the sub-pixel comprising:

a switching element (see TFT); and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the pixel electrode;

a control terminal of the switching element is electrically connected to the gate signal line; and

each switching element in one of the pixels is electrically connected to different one of the gate signal lines.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 6, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising n sub-pixels, each sub-pixel comprising:

a switching element; and

a pixel electrode,

wherein:

n lines of the gate signal lines are corresponding to one pixel row;

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the pixel electrode;

a control terminal of the switching element is electrically connected to the gate signal line; and

each switching element in one of the pixels is electrically connected to corresponding one of the n lines of the gate signal lines.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 7, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixel arranged in matrix, each of the pixels comprising:

a switching element;

a driver element; and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the driver element;

a control terminal of the switching element is electrically connected to the gate signal line; and

the driver element is electrically connected to the pixel electrode.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 8, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising a plurality of sub-pixels, each of the sub-pixels comprising:

a switching element; and

a driver element; and a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line,

an output terminal of the switching element is electrically connected to the driver element;

a control terminal of the switching element is electrically connected to the gate signal line; and

the driver element is electrically connected to the pixel electrode.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 9, Tanaka et al. discloses in fig. 12, a display device comprising:

a

plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (x1-Xn); and

a plurality of pixels arranged in matrix comprising a plurality of sub-pixels, each of the sub-pixels comprising:

a switching element;

a driver element; and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the driver element;

a control terminal of the switching element is electrically connected to the gate signal line;

the driver element is electrically connected to the pixel electrode; and

each switching element in one of the pixels is electrically connected to different one of the source signal lines.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 10, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines X1-Xn); and

a plurality of pixels arranged in matrix comprising n sub-pixels, each of the sub-pixels comprising:

a switching element;

a driver element; and

a pixel electrode;

wherein:

n lines of the source signal lines are corresponding to one pixel column

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the driver element;

a control terminal of the switching element is electrically connected to the gate signal line;

the driver element is electrically connected to the pixel electrode; and

each switching element in one of the pixels is electrically connected to corresponding on~ of the n lines of the gate signal lines.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 11, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising a plurality of sub-pixels, each of the sub-pixels comprising:

a switching element;

a driver element; and

a pixel electrode,

wherein:

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the driver element;

a control terminal of the switching element is electrically connected to the gate signal line;

the driver element is electrically connected to the pixel electrode; and

each switching element in one of the pixels is electrically connected to different one of the gate signal lines.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

As to claim 12, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising n sub-pixels, each of the sub-pixels comprising:

a switching element;

a driver element; and

a pixel electrode,

wherein:

n lines of the gate signal lines are corresponding to one pixel row;

an input terminal of the switching element is electrically connected to the source signal line;

an output terminal of the switching element is electrically connected to the driver element;

a control terminal of the switching element is electrically connected to the gate signal line;

the driver element is electrically connected to the pixel electrode; and

each switching element in one of the pixels is electrically connected to any one of the n lines of the gate signal lines.

As to claim 13, Tanaka et al. discloses further, wherein a ferroelectric memory is utilized as the nonvolatile memory element (see 0032).

As to claim 14, Tanaka et al. discloses further, wherein a thin film transistor is utilized as the switching element.

As to claim 15, Tanaka et al. discloses further, a display device as discussed, wherein the source signal line driver circuit (Y1-Ym) is formed on the same substrate as the pixel.

As to claims 16, 19,Tanaka et al. discloses further, a display device as discussed, wherein the gate signal line driver circuit is formed on the same substrate as the pixel and electric apparatuses applied to the claims 1-12.

As to claim 20, Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix, each of the pixels comprising:

a first switching element(a first TFT);

a second switching element (a second TFT);

a capacitor element (C); and

a pixel electrode,

wherein:

an input terminal of the first switching element is electrically connected to the source signal line; an output terminal of the second switching element is electrically connected to an input terminal of the second switching element and the pixel electrode;

a control terminal of the first switching element is electrically connected to the gate signal line; and

the second switching element is selectively connected to one of the capacitor element.

However, Tanaka et al. does not disclose in fig. 12, a nonvolatile memory element, and an output terminal of the switching element is electrically connected to the nonvolatile memory element.

Tanaka et al. discloses in fig. 1, a nonvolatile memory element (see nonvolatile 3) and an output terminal of the switching element (of TFT 2) is electrically connected to nonvolatile memory element (3) as discussed above.

4. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 2001/007447) in view of Miyawaki et al. (US 6,166,792).

Tanaka et al. discloses in fig. 12, a display device comprising:

a plurality of source signal lines (Y1-Ym);

a plurality of gate signal lines (X1-Xn); and

a plurality of pixels arranged in matrix comprising n sub-pixels, each of the sub-pixels comprising:

a switching element;

a driver element; and

a pixel electrode as discussed above. However, Tanaka et al. does not disclose that wherein the source signal line driver circuit is configured with unipolar transistors.

Miyawaki et al. discloses in fig. 3, the sampling switches 33 at source signal line driver circuit comprising unipolar transistors (see col. 10, lines 45-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the source signal line driver circuit is figured with unipolar Miyawaki et

transistors as taught by Miyawaki et al. in to the system of Tanaka et al. for producing the claimed invention because this would provide this arrangement, images of higher quality can be displayed on the screen of the display panel (see col. 10, lines 58-62).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kimnhung Nguyen
January 8, 2007

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